

REMARKS

The drawings have been objected to. The specification has been amended to clarify description of the following reference characters: C1, C3, C5-C10, ACT, RA, CA, D1, D2, CSL0, CSL1, CSL2, 12, 14, 15, 41, 42, 43, 45, 46, 62, 75, PtWR1, PtWR2, PtWR3, 206 and 301. With regard to reference character WRITE, WRITE is described in the specification as filed at least at page 9, line 21. With regard to reference character D0, D0 is described in the specification as filed at least at page 9, lines 22-23. With regard to reference character D3, D3 is described in the specification as filed at least at page 10, lines 14-15. With regard to reference characters Y0, Y1, Y2 and Y3, these are described in the specification as filed at least at page 10, lines 4-6. With regard to reference character CSL3, CSL3 is described in the specification as filed at least at page 11, lines 11-12. With regard to reference character 74, 74 is described in the specification as filed at least at page 14, lines 23-26. The amendments to the specification with regard to reference characters ACT, RA, CA, PtWR1, PtWR2, and PtWR3 correct clerical errors. The remaining amendments to the specification merely specifically refer to reference characters in the drawings which were not previously referenced in the specification. No new matter is added by the above clarifying amendments to the specification. In view of the amendments to the specification and the foregoing remarks, it is believed that the objection to the drawings is overcome, and reconsideration is requested.

The claims are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The specification has been amended to include description of the following reference characters: C1, C3, C5-C10, ACT, RA, CA, D1, D2, CSL0, CSL1, CSL2, 12, 14, 15, 41, 42, 43, 45, 46, 62, 75, PtWR1, PtWR2, PtWR3, 206 and 301. It is believed that the objection to the claims is overcome, and reconsideration is requested.

Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidaka (U.S. Patent Number 6,172,918). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-23, a semiconductor device includes switching devices activated by a column selection line signal provided during a write time and a write recovery time for electrically connecting a data line and a complementary data line to a bit

line and a complementary bit line. The semiconductor device further includes a write driver for supplying a write data voltage to the data line and the complementary data line during the write time and resupplying the last write data voltage to the data line and the complementary data line during the write recovery time.

Claims 1-23 are amended to clarify certain features of the invention. Specifically, the claims are amended to recite that the semiconductor device includes switching devices activated by the column selection line signal provided during the write time and the write recovery time and the write driver for supplying a write data voltage to the data line and the complementary data line during the write time and resupplying the last write data voltage to the data line and the complementary data line during the write recovery time.

In the present invention as claimed in claims 24-31, a method of controlling a semiconductor device includes writing a data voltage into a memory cell array during a write time and providing a column selection line signal during a write recovery time and rewriting the last data voltage during the write recovery time.

Claims 24-31 are amended to clarify certain features of the invention. Specifically, the claims are amended to recite that the method of controlling the semiconductor device includes writing the data voltage into the memory cell array during the write time and providing the column selection line signal during the write recovery time and rewriting the last data voltage during the write recovery time.

Hidaka discloses a semiconductor memory device for reducing the time required for reading of data and reducing the write recovery time. Hidaka fails to teach or suggest that a semiconductor device includes switching devices activated by a column selection line signal provided during a write time and a write recovery time and a write driver for supplying a write data voltage to a data line and a complementary data line during the write time and resupplying the last write data voltage to the data line and the complementary data line during the write recovery time, as claimed in claims 1-23. Hidaka further fails to teach or suggest that a method for controlling a semiconductor device includes writing a data voltage into a memory cell array during a write time and providing a column selection line signal during a write recovery time and rewriting the last data voltage during the write recovery time, as claimed in claims 24-31.

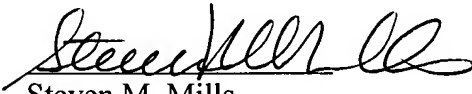
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Hidaka fails to teach or suggest the elements of the invention set forth in the amended claims. Therefore, it is believed that the amended claims are allowable over the cited reference, and reconsideration of the rejection of claims 1-31 under 35 U.S.C. 103(a) as being unpatentable over Hidaka is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 10/25/05
Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
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Steven M. Mills
Registration Number 36,610
Attorney for Applicants